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Docket No.: 042390.P5512

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Franklin M. Baez

Application No.: 09/148,392

Filed: September 4, 1998

For: SELECTING DESIGN POINTS ON PARAMETER FUNCTIONS HAVING FIRST SUM OF CONSTRAINT SET AND SECOND SUM OF OPTIMIZING SET TO IMPROVE SECOND SUM WITHIN DESIGN CONSTRAINTS

Examiner: William D. Thomson

Art Group: 2123

SUPPLEMENTAL APPEAL BRIEF

Assistant Commissioner for Patents
Washington, DC 20231-9999

Dear Sir:

Applicant submits the following Supplemental Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. This Supplemental Appeal Brief amends the Appeal Brief filed on September 9, 2002 to correct a mistake in the Grouping of Claims section. This Supplemental Appeal Brief is submitted concurrently with the Reply Brief.

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IX. APPENDIX 12

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Intel Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellants, the appellants' legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 and 22-29 of the present application are pending and remain rejected. The Applicant hereby appeals the rejection of claims 1-20 and 22-29.

IV. STATUS OF AMENDMENTS

The Applicant filed an amendment on June 12, 2002, in response to a Final Office Action issued by the Examiner on April 9, 2002. In response to the June 12, 2002 amendment, the Examiner issued an Advisory Action on July 3, 2002. The Applicant filed a Notice of Appeal from the Advisory Action issued by the Examiner on July 9, 2002.

V. SUMMARY OF INVENTION

The present invention is a method and computer program product for determining the optimal values of the design parameters of a circuit block. Parameter functions relating the design parameters for circuits in the circuit block are created. Based on these parameter functions, the design parameters are optimized to satisfy the design constraints.[1]

The design constraints are usually dictated by the system requirements and specifications. Examples of the design constraints include propagation delay, power consumption, packaging, number of input/ output (I/O) lines, etc. The design constraints are typically imposed on one or more design parameters, while leaving other parameters to

[1] See specification, page 4, lines 2-6

be optimized to achieve high performance[2]. The design parameters, therefore, are divided into two parameter sets: a constraint set and an optimizing set. The "constraint set" includes constraint parameters which are the parameters that have to meet the design constraints. The "optimizing set" includes the optimizing parameters which are the parameters that need to be optimized[3].

The relationship between the constraint parameters and the optimizing parameters is described by a parameter function. A "parameter function" describes the variation of one parameter as a function of another parameter. For example, a parameter function may describe the variation of the power consumption as a function of the delay. The variation of one parameter as a function of another is typically caused by a configuration of the circuit such as the size of the transistors, the choice of circuit technology (e.g., domino versus static), etc. A configuration of the circuit that gives rise to the particular values of the design parameters corresponds to a design point[4].

A system, a subsystem, a module or a functional block may consist of a number of circuits. Each circuit is characterized by a parameter function. Optimizing the design of a subsystem or functional block involves a trade-off consideration of all the parameter functions of all the individual circuits of the subsystem or functional block[5]. For a parameter function of a given circuit, there are many design points corresponding to different circuit configurations. Therefore, optimizing a subsystem or functional block involves the selection of the design points on the parameter functions that provide the optimal values of the optimizing parameters and acceptable values of the constraint parameters[6].

The design optimization phase includes the generation of the power-delay curves for the individual circuit elements. Then a trade-off analysis is performed on these power-delay curves. Each power-delay curve has several design points. Each design point corresponds to a design configuration of the individual circuit element[7]. In one embodiment, the design configuration is the transistor size characterized by a scale factor. The design optimization phase begins with a set of initial design points on the power-delay curves. These initial design points correspond to a composite delay that meets the

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[2] See specification, page 6, lines 20-25
[3] See specification, page 7, lines 1-5
[4] See specification, page 7, lines 9-17
[5] See specification, page 7, lines 18-22
[6] See specification, page 7, lines 22-26; page 8, line 1

specified timing constraint. The optimization process then proceeds to iteratively determine the new set of design points on the power-delay curves such that the specified timing constraint remains met while the total power is reduced[8].

A circuit subsystem may include several circuit blocks. Each of the circuit blocks has a power-delay curve on which an initial design point and a new design point are selected[9]. The initial design points have a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints[10]. The new design points are selected such that the second sum is improved within the design constraints[11].

The optimization process can be applied for different circuit configurations. For example, a circuit block can be designed using a static circuit technology or a dynamic (e.g., domino) circuit technology[12]. A different technology is selected if the improved optimizing parameter is better than the previous one.[13]

VI. ISSUE

The issue is:

(i) whether claims 1-20 and 22-29 are unpatentable under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,838,947 issued to Sarin ("Sarin") or U.S. Patent No. 5, 880,967 issued to Jyu et al. ("Jyu") or United States Patent No. 5,666,2888 issued to Jones et al. ("Jones") or U.S. Patent No. 5,835,380 issued to Roething ("Roething"); or under 35 U.S.C. §102(a) as being anticipated by Roething; or under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,619,420 issued to Breid ("Breid") and Applicant's own admittance (AOA)

VII. GROUPING OF CLAIMS

Applicant contends that the claims of the present invention form into two groups. Group 1 includes claims 1-20 and 22-27 and Group 2 includes claims 28-29.

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[7] See specification, page 19, lines 1-5
[8] See specification, page 19, lines 5-11
[9] See specification, page 19, lines 12-25; Figures 6A-6D.
[10] See specification, page 20, lines 21-24
[11] See specification, page 21, lines 1-4
[12] See specification, page 21, lines 10-15

VIII. ARGUMENTS

A. Claims 1-20 and 22-29 Are Not Anticipated By Sarin, Jyu, Jones, Roethig, and Breid and Applicant's Own Admittance.

In the Office Action, the Examiner rejected Claims 1-20 and 22-29 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,838,947 issued to Sarin ("Sarin") or U.S. Patent No. 5, 880,967 issued to Jyu et al. ("Jyu") or United States Patent No. 5,666,2888 issued to Jones et al. ("Jones") or U.S. Patent No. 5,835,380 issued to Roething ("Roething"). The Examiner also rejected Claims 1-20 and 22-29 under 35 U.S.C. § 102(a) as anticipated by Roething, and rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,619,420 issued to Breid ("Breid") and Applicant's own admittance (AOA) of the use of integrated commercial packages of Pathmill, Powermill, AMPS and ISPICE, iVGEN and ISPEC2. Applicant respectfully traverses the rejections for the following reasons.

Sarin discloses a modeling, characterization and simulation of integrated circuit power behavior. Sarin merely discloses a method to simulate power behavior of digital VLSI MOS circuit at the gate level (Sarin, col. 2, lines 14-16). For each state-vector, power consumption measurements are carried out for different conditions of input ramp and output load (Sarin, col. 2, lines 22-24). A power dissipation model is used to predict power behavior (Sarin, col. 9, lines 23-36).

Jyu discloses a minimization of circuit delay and power through transistor sizing using an autosizing engine. Jyu discloses design goals commands including a requirement mode. In requirement mode, two requirement parameters may be specified: delay and power. If one requirement is specified, the engine will first satisfy the specified requirement and then minimize the other (Jyu, col. 10, lines 56-62). The autosizing engine performs initial search and select by simulating a circuit retrieved from netlist files (Jyu, col. 13, lines 26-37). Then, the engine generates user-specified scaling and changing circuits for power simulation and delay analysis (Jyu, col. 14, lines 53-69). The engine merely sizes up and down a transistor.

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[13] See specification, page 17, lines 6-24; page 18, lines 1-5; Figure 4

Jones discloses a method and apparatus for designing an integrated circuit. Jones discloses providing a behavioral model and an initial library of logic cells to a design synthesis tool (Jones, col. 3, lines 30-33). Cell strengths are altered by altering specific sizes of transistors in the gate schematic net list (Jones, col. 3, lines 41-42). The size alteration is used to achieve speed path constraints while minimizing area or power impact (Jones, col. 3, lines 42-43). Then, a new hybrid library must be generated taking into account the changes made by these optimizations (Jones, col. 3, lines 61-63).

Roethig discloses a simulation based extractor or expected waveforms for gate-level power analysis tool. Roethig discloses performing a simulation and then calculating power information from a database (Roethig, col. 4, lines 47-50). A power analysis tool includes a power calculator that converts average current, propagation delay, and intrinsic delay into positive and negative load currents for a cell (Roethig, col. 3, lines 10-13)

Breid discloses a semiconductor cell having a variable transistor width. A cell library definition includes a transistor width input variable which allows transistors in the cell to be sized during the layout process to eliminate timing violations and to minimize power consumption (Breid, col. 3, lines 54-59)

AOA merely discloses the use of integrated commercial packages of Pathmill, Powermill, AMPS and ISPICE, iVGEN and ISPEC2 in the specification, not in the prior art discussion. These tools are merely individual tools for design analysis of power, verification of timing parameters, and transistor-level circuit analysis.

Sarin, Jyu, Jones, Roethig, and Breid and AOA, taken alone or in any combination, do not disclose, either expressly or inherently, suggest, or render obvious: (1) selecting initial design points having a first sum of the constraint set and a second sum of the optimizing set, (2) selecting the new design points such that the second sum is improved within the design constraints, and (3) selecting a first technology if the first improved optimizing parameter is better than the second improved optimizing parameter, and else selecting a second technology.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the

...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Since the Examiner failed to show that Sarin, Jyu, Jones, Roethig, and Breid teaches or discloses any one of the above elements, the rejection under 35 U.S.C. §102 is improper.

In the Office Action, the Examiner stated that "Sarin and Jyu et al. and Roethig and Breid explicitly teach a constraint parameter set that is the propagation delay and an optimizing parameter set that is the power consumption." However, even assuming that this is true, none of the cited prior art references teach "selecting initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints."

The Examiner stated that Applicant is merely summing the sets of data to see if it meets and/or improves the design. However, none of the cited prior art references teaches or suggests a parameter function having a first sum of the constraint set and a second sum of the optimizing set.

The Examiner further stated that Applicant's arguments amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. However, it is the Examiner who made a general allegation without specifically pointing out the column number and the line number of each of the cited references that teach: (1) first sum of constraint set, (2) second sum of optimizing set, (3) selecting initial design points such that first sum satisfies the design constraints, (4) selecting new design points such that the second sum is improved within the design constraints, (5) selecting the first technology if the first improved optimizing parameter is better than the second improved optimizing parameter, else selecting the second technology.

Where a claim is refused for any reason relating to the merits thereof it should be "rejected" and the ground of rejection fully and clearly stated. See MPEP 707.07(d). Where the applicant traverses an objection, the Examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it. See MPEP 707.07(f). An omnibus rejection of the claim "on the reference and for reasons of record" is stereotyped and usually not informative and should therefore be avoided. See MPEP 707.07(d).

The Examiner repeated the rejection without taking note of the Applicant's arguments and without answering the substance of Applicant's arguments as presented in the response previously filed. The MPEP requires that the Examiner's action will be complete as to all matters. 37 CRF 1.104; MPEP 707.07.

B. <u>The Examiner's Holding Of Non-Persuasive Argument Is Not Only Form Over Substance, But Also Erroneous.</u>

In the Advisory Action dated July 3, 2002, the Examiner stated "[a]pplicant has mis[s]-stated sections of the MPEP and attempted to quote sections that are not pertinent and therefore non-persuasive. An example is MPEP 706.2(j) relates to 103 rejections not to 102 rejections, as was the instant case." Applicant respectfully disagrees.

The two quotes that the Examiner refer to are copied below for ease of reference:

> "It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply. See MPEP 706.02(j)."

> "The Examiner should set forth in the Office Action the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate. See MPEP 706.02(j). The goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of a patentability and otherwise reply completely at the earliest opportunity. See MPEP 706."

Although these paragraphs are taken under the section discussing a 103 rejection, the contents of the paragraphs are well applicable to the 102 rejections because they are related to showing of evidence in the prior art reference. They are not related to the substantive rejection. In a 102 rejection, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Therefore, the burden of showing evidence in the prior art reference for a 102 rejection is heavier than for a 103 rejection. The paragraphs under MPEP 706.2(j) are quoted to show that even for a 103 rejection, the Examiner must properly communicate the basis for a rejection and set forth with reference to the relevant column or page number(s) and line number(s).

Referencing a paragraph in a section discussing a 103 rejection does not preclude the applicability of that paragraph for other type of rejections. For example, the MPEP 707.07(d) discusses the language to be used in rejecting claims. This section is applicable

to all types of rejections even though it refers to MPEP 706.02(i), (j) and (m) which are sections discussing 103 rejections.

By arguing that the quoted paragraphs are not pertinent and therefore non-persuasive, the Examiner seems to state that for a 102 rejection: (1) it is not important for an examiner to properly communicate the basis for a rejection, and (2) the Examiner should not set forth the relevant teachings with reference to the relevant column or page number(s) and line number(s). Clearly, this is against the guidelines and spirit of the process of examining a patent application.

Accordingly, Applicant submits that the Examiner's holding of non-persuasive argument is not only form over substance, but also erroneous.

Therefore, Applicant believes that independent claims 1, 11, 22, and 28 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. §102(a)(b)(e) be withdrawn.

C. Conclusion

The Federal Circuit stated that to anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Neither one of Sarin, Jyu, Jones, Roethig, and Breid and AOA discloses, suggest, or render obvious: (1) first sum of constraint set, (2) second sum of optimizing set, (3) selecting initial design points such that first sum satisfies the design constraints, (4) selecting new design points such that the second sum is improved within the design constraints, (5) selecting the first technology if the first improved optimizing parameter is better than the second improved optimizing parameter, else selecting the second technology. As a result, none of the cited references discloses, suggests, or renders obvious the present invention as recited in claims 1-20 and 22-29.

Applicant respectfully request that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are neither anticipated or rendered obvious by the prior art.

Respectfully submitted,

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Dated: February 3, 2003

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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (THREE TIMES AMENDED) A method comprising:

(a) creating parameter functions for a plurality of circuits in a subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits, the parameter functions representing a relationship among design parameters of the subsystem, the design parameters including constraint and optimizing sets;

(b) selecting initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and

(c) selecting new design points on the parameter functions such that the second sum is improved within the design constraints.

2. The method of claim 1 wherein the creating the parameter functions comprises:

(a1) configuring each circuit of the plurality of circuits; and

(a2) generating values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions.

3. (AMENDED) The method of claim 2 wherein the constraint set includes constraint parameters having values selectable to meet the design constraints and the optimizing set includes optimizing parameters having values to be optimized.

4. (AMENDED) The method of claim 3 wherein selecting the new design points comprises:

(c1) selecting values of the constraint parameters to meet the design constraints;

(c2) determining values of the optimizing parameters corresponding to the selected values of the constraint parameters based on the parameter functions; and

(c3) iterating c(1) and (c2) until values of the optimizing parameters are within a predetermined optimal range.

5. The method of claim 3 wherein the constraint parameters include a delay parameter and the optimizing parameters include a power parameter.

6. The method of claim 5 wherein the design constraints include a delay constraint.

7. The method of claim 6 wherein (a1) comprises:
sizing components in each circuit.

8. The method of claim 6 wherein (a1) comprises:
selecting a design technology for each circuit, the design technology being one of static and dynamic technologies.

9. The method of claim 7 wherein (a2) comprises:
(a21) generating a circuit netlist representing the configured circuit;
(a22) generating a timing file based on the circuit netlist using a circuit critical path;
(a23) determining power of the configured circuit based on the circuit netlist;
(a24) calculating timing values by using a timing simulator; and
(a25) calculating power values by using a power estimator.

10. The method of claim 9 wherein selecting the new design points comprises:
(c1) selecting values of the delay parameter within the delay constraint;
(c2) determining values of the power parameter corresponding to the selected values of the delay parameter based on the parameter function; and
(c3) iterating (c1) and (c2) until values of the power parameter are within a predetermined optimal range.

11. (TWICE AMENDED) A machine readable medium having embodied thereon a computer program for processing by a machine, the computer program comprising:

(a) a first code segment to create parameter functions for a plurality of circuits in a subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits, the parameter functions representing a relationship among design parameters of the subsystem, the design parameters including constraint and optimizing sets;

(b) a second code segment to select initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and

(c) a third code segment to select new design points on the parameter functions such that the second sum is improved within the design constraints.

12. (AMENDED) The machine readable medium of claim 11 wherein the first code segment comprises:

(a1) a code segment to configure each circuit of the plurality of circuits; and

(a2) a code segment to generate values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions.

13. (AMENDED) The machine readable medium of claim 12 wherein the constraint set includes constraint parameters having values selectable to meet the design constraints and the optimizing set includes optimizing parameters having values to be optimized.

14. (AMENDED) The machine readable medium of claim 13 wherein the third code segment comprises:

(c1) a code segment to select values of the constraint parameters to meet the design constraints;

(c2) a code segment to determine values of the optimizing parameters corresponding to the selected values of the constraint parameters based on the parameter functions; and

(c3) a code segment to iterate (c1) and (c2) until values of the optimizing parameters are within a predetermined optimal range.

15. The machine readable medium of claim 13 wherein the constraint parameters include a delay parameter and the optimizing parameters include a power parameter.

16. The machine readable medium of claim 15 wherein the design constraints include a delay constraint.

17. (AMENDED) The machine readable medium of claim 16 wherein (a1) comprises:

a code segment to size components in each circuit.

18. (AMENDED) The machine readable medium of claim 16 wherein (a1) comprises:

a code segment to select a design technology for each circuit, the design technology being one of static and dynamic technologies.

19. (AMENDED) The machine readable medium of claim 18 wherein (a2) comprises:

(a21) a code segment to generate a circuit netlist representing the configured circuit;

(a22) a code segment to generate a timing file based on the circuit netlist using a circuit critical path;

(a23) a code segment to determine power vectors of the configured circuit based on the circuit netlist;

(a24) a code segment to calculate timing values; and

(a25) a code segment to calculate power values.

20. (AMENDED) The machine readable medium of claim 19 wherein the third code segment comprises:

(c1) a code segment to select values of the delay parameter within the delay constraints;

(c2) a code segment to determine values of the power parameter corresponding to the selected values of the delay parameter based on the parameter function; and

(c3) a code segment to iterate (c1) and (c2) until values of the power parameter are within a predetermined optimal range.

21. (CANCELLED)

22. (THREE TIMES AMENDED) A system comprising:

a memory for storing program instructions;

a processor coupled to the memory to execute the program instructions, the program instructions when executed by the processor interacting with tools provided by a design environment causing the processor to at least

(a) create parameter functions for a plurality of circuits in a subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits, the parameter functions representing a relationship among design parameters of the subsystem, the design parameters including constraint and optimizing sets,

(b) select initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and

(c) select new design points on the parameter functions such that the second sum is improved within the design constraints.

23. (AMENDED) The system of claim 22 wherein the program instructions causing the processor to create the parameter functions causes the processor to:

(a1) configure each circuit of the plurality of circuits; and

(a2) generate values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions.

24. (AMENDED) The system of claim 22 wherein the constraint set includes constraint parameters having values selectable to meet the design constraints and the optimizing set includes optimizing parameters having values to be optimized.

25. (AMENDED) The system of claim 24 wherein the program instructions causing the processor to select the new design points causes the processor to:

(c1) select values of the constraint parameters to meet the design constraints;

(c2) determine values of the optimizing parameters corresponding to the selected values of the constraint parameters based on the parameter functions; and

(c3) iterate (c1) and (c2) until values of the optimizing parameters are within a predetermined optimal range.

26. The system of claim 24 wherein the constraint parameters include a delay parameter and the optimizing parameters include a power parameter.

27. The system of claim 26 wherein the design constraints include a delay constraint.

28. A method comprising:

(a) generating first and second parameter functions for a circuit corresponding to first and second technologies, each of the first and second parameter functions relating a constraint parameter and an optimizing parameter;

(b) selecting a first initial design point and a first new design point on the first parameter function such that the first new design point corresponds to a first improved optimizing parameter within a design constraint;

(c) selecting a second initial design point and a second new design point on the second parameter function such that the second new design point corresponds to a second improved optimizing parameter within the design constraint; and

(d) selecting the first technology if the first improved optimizing parameter is better than the second improved optimizing parameter, else selecting the second technology.

29. The method of claim 28 wherein the first technology is a dynamic technology and the second technology is a static technology.

29. The method of claim 28 wherein the first technology is a dynamic technology and the second technology is a static technology.